REMARKS

The following remarks are made in response to the Office Action mailed May 7, 2007. Claims 1-24 were rejected. Claims 1-24 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 103

The Examiner rejected claims 1-24 under 35 U.S.C. § 103(a) as being unpatentable over the Arora U.S. Patent No. 6,393,556 in view of the Banning et al. U.S. Patent No. 6,363,336.

Applicants submit that the Arora Patent and the Banning Patent, either alone, or in combination, fail to teach or suggest the invention of independent claims 1, 6, 12, 17, and 23.

The Arora Patent discloses changing a privilege level in a processor configured to pipeline instructions. The processor includes a first memory storing an architectural privilege level that is set at a first privilege level, a second memory storing a plurality of instructions, and a pipeline including a plurality of processing stages. A first instruction is fetched from the memory and a determination is made whether the first instruction requires the first privilege level be changed to a second privilege level, and in response thereto, any subsequent instructions are flushed from the pipeline before recording the second privilege level in the first memory. (Abstract).

In the Arora Patent, the processor 30 maintains a "current privilege level" (CPL) 38 in a memory storage device. The CPL is maintained in the processor's register set. The operating system sets the CPL to prevent the user from performing dangerous or insecure operations. If the pipeline 30 is currently processing an application program instruction, a prior instruction would have set the CPL 38 to the proper privilege level. If an instruction requiring a higher privilege level follows the current instruction, an instruction, such as an "enter privilege code" (EPC) instruction, that directs the processor to change the privilege level of the CPL must first be processed to increase the privilege level. (Col. 4, lines 13-27).

In the Arora Patent, after decoding an instruction directing the processor to change the CPL 38 from a first to a second privilege level, the processor compares the second privilege level to the CPL 38. (Col. 6, lines 27-31). The processor will compare the CPL 38 with the

privilege level specified in the EPC instruction. If the EPC instruction directs the processor to change the CPL 38 to a higher privilege level, the processor flushes any instructions in the pipeline subsequent to the EPC instruction, and continues processing the EPC instruction. When the EPC instruction is retired, the CPL 38 privilege level is increased. If the EPC instruction specifies a privilege level lower than or the same as the CPL 38, the processor will issue a fault. (Col. 6, lines 46-59).

The Banning Patent discloses a method for determining if writes to a memory page are directed to target instructions which have been translated to host instructions in a computer which translates instructions for a target instruction set to a host instruction set, including the steps of detecting a write to a memory page storing target instructions which have been translated to host instructions, detecting whether a sub-area of the memory page to which the write is addressed stores target instructions which have been translated, and invalidating host instructions translated from addressed target instructions. (Abstract).

The Arora Patent and the Banning Patent, either alone, or in combination, fail to teach or suggest **performing a privilege promotion instruction by the operating system, the privilege promotion instruction being stored in a first page of memory not writeable by application instructions at a first privilege level, the privilege promotion instruction including: reading a stored previous privilege level state; comparing the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a second privilege level which is higher than the first privilege level** as recited in independent method claim 1.

The Examiner submits that the Arora Patent discloses "the privilege promotion instruction being stored in a first page of memory (instruction memory 36 storing a plurality of instructions... see Figure 2). (Office Action, page 5). The Examiner admits that the Arora Patent does not teach the instruction memory 36 including a page of memory not writeable by application instructions at a first privilege level. The Examiner submits that the Banning Patent discloses an instruction memory where memory pages marked with a T bit are protected and if a write is attempted, an exception is generated. The Examiner further

submits that in this system, the T bit provides the protection so that the memory page is not writeable at the first privilege level. (Office Action, page 6).

Instruction memory 36 of Figure 2 of the Arora Patent is a cache memory for storing instructions that are processed in the pipeline 32. A cache memory is a portion of memory that operates faster than main memory. The first time an instruction is executed, it must be loaded from the relatively slow main memory. Recently-accessed memory locations are saved in the cache in case they are needed again, so each instruction will be saved in the cache after being loaded from the memory the first time. (Col. 3, lines 24-35). Instruction memory 36 does not include a first page of memory not writeable by application instructions at a first privilege level. Instruction memory 36 is a cache memory where all instructions are stored for execution. The Arora Patent discloses that a typical pipeline 32 includes a stage during which instructions are fetched from the memory 36. (Col. 3, lines 44-46). The EPC instruction 111 is fetched from the instruction memory 36. (Col. 4, lines 50-51).

The Banning Patent also fails to teach or suggest a *privilege promotion instruction* being stored in a first page of memory not writeable by application instructions at a first privilege level. In addition, there is no teaching or suggestion for one skilled in the art to combine the cache memory of the Arora Patent with the T bit system of the Banning Patent. Cache memories store data temporarily, therefore one skilled in the art would not implement the T bit system of the Banning Patent to protect instructions temporarily stored in the cache memory of the Arora Patent from being overwritten. Therefore, the Arora Patent and the Banning Patent fail to teach or suggest *the privilege promotion instruction being stored in a first page of memory not writeable by application instructions at a first privilege level.*

The Examiner states that the claim 1 limitation of reading a stored previous privilege level state is disclosed by the Arora Patent at column 4, lines 19-22 by register CPL 38, which stores the privilege level set by a previous instruction. (Office Action, page 5). The Examiner also states that comparing the read previous privilege level state to the current privilege level is disclosed in column 6, lines 46-49 of the Arora Patent. (Office Action, pages 5-6). Further, the Examiner also states that the privilege level stored in CPL 38 is the previous privilege level since it represents a previous instruction, while the privilege level related to the EPC is the current privilege level since it represents the current instruction.

(Office Action, page 6). In addition, the Examiner states that "at the moment of comparison, the privilege level of EPC is the privilege level necessary for the instruction that is currently being prepared for execution in the system (instruction requiring a higher priority level follows in the pipeline), thus it is a current privilege level. Also, at the moment of comparison, the CPL is the previous privilege level because it was the privilege level set by a prior instruction (Col. 4, lines 19-28), and it is the privilege level that was necessary for the execution of an instruction that was executed previous to the instruction corresponding to the EPC." (Office Action, page 3).

The Arora Patent states, however, that "[i]f an instruction requiring a higher privilege level follows the *current* instruction, an instruction, such as an 'enter privilege code' ('EPC') instruction, that directs the processor to change the privilege level of the architectural CPL must first be processed to increase the privilege level." (Col. 4, lines 22-27). The privilege level stored in CPL 38 is not updated until after the EPC instruction is executed. The privilege level stored in CPL 38 remains the current privilege level during the execution of the EPC instruction.

The cited text of the Arora Patent discloses comparing the architectural CPL with the privilege level specified in the EPC instruction. (Col. 6, lines 46-49). The Arora Patent fails to disclose the claim 1 limitations of *reading a stored previous privilege level state* and *comparing the read previous privilege level state to the current privilege level*. In the Arora Patent, a previous privilege level state is not stored and therefore cannot be read. The privilege level stored in CPL 38 is never the previous privilege level as submitted by the Examiner. CPL 38 remains the current privilege level until an EPC instruction is retired.

The Arora Patent also discloses that the CPL is compared to the privilege level specified in the EPC instruction. In contrast, claim 1 requires comparing the *read previous privilege level state* to the *current privilege level*. The privilege level of the EPC instruction does not teach or suggest the current privilege level. Rather, the EPC instruction directs the processor to change the privilege level of the CPL. (Col. 4, lines 24-26). The EPC instruction provides a potential future privilege level, not the current privilege level. The Arora Patent discloses that an EPC instruction *eventually may* cause the processor 30 to change the architectural CPL 38 to a second privilege level. (Col. 4, lines 56-58).

The Examiner states that the claim 1 limitations of "if a previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a second privilege level which is higher than the first privilege level" are disclosed by the Arora Patent "since the EPC instruction directs the processor to change the architectural privilege level to a higher privilege level . . .". (". . . increase the architectural privilege level from privilege level 3 to privilege level 0"). (Office Action, page 6). The Examiner further states that in comparing privilege levels, the stored privilege level (stored in CPL 38) must be read in the comparison process. (Office Action, page 6).

The Arora Patent discloses raising the current architectural CPL to the privilege level specified in the EPC instruction. (Col. 6, lines 46-49). The Arora Patent, however, does not disclose the claim 1 limitation of promoting the current privilege level to a second privilege level which is higher than the first privilege level if the previous privilege level state is equal to or less privileged than the current privilege level.

Claim 1 recites if the *previous privilege level state* is *equal* to or *less privileged* than the *current privilege level*, promoting the current privilege level. In contrast, the Examiner states that the Arora Patent discloses increasing the *current privilege level* if the privilege level of the *CPL* is *lower* than the privilege level of the *EPC*. The Arora Patent discloses if the EPC instruction specifies a privilege level lower than, *or the same as*, the architectural CPL, the processor will issue a fault rather than promote the CPL. (Col. 6, lines 56-59). In addition, the Examiner states that the privilege level of the EPC instruction discloses the current privilege level state and the CPL discloses the stored previous privilege level state. (Office Action, page 3). Further, the Examiner states that the privilege level of the EPC instruction is the privilege level necessary for the instruction that is currently being prepared for execution in the system, thus it is a current privilege level; and that the CPL is the previous privilege level because it was the privilege level necessary for the execution of a previous instruction. (Office Action, page 3). Therefore, based on the Examiner's interpretation, claim 1 would recite if the CPL is equal to or less privileged than the privilege level of the EPC instruction, promoting the current privilege level. The CPL, however, is the current privilege level, not the previous privilege level state, and the privilege level of the EPC instruction is a future privilege level, not the current privilege level as submitted by the

Examiner. The CPL in the Arora Patent is not increased to the privilege level of the EPC instruction until the EPC instruction is retired. (Col. 6, lines 54-56).

In view of the above, Applicants believe independent claim 1 to be allowable over the Arora Patent and the Banning Patent. Dependent claims 2-5 further define patentably distinct independent claim 1. Accordingly, dependent claims 2-5 are also believed to be allowable over the Arora Patent and the Banning Patent.

The Arora Patent also fails to teach or suggest **performing a call instruction to a second page of memory not writeable by the application instructions at the first privilege level, the call instruction including: storing a return address to the first page of memory; and storing the first privilege level in a previous privilege level state; and performing a privilege promotion instruction by the operating system, the privilege promotion instruction being stored in the second page of memory, the privilege promotion instruction including: reading the stored previous privilege level state; comparing the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a second privilege level which is higher than the first privilege level** as recited in independent method claim 6.

For similar reasons as discussed above with reference to independent claim 1, the Arora Patent and the Banning Patent, either alone, or in combination, fail to teach or suggest the above limitations of claim 6, which are similar to the above limitations of claim 1.

In addition, the Arora Patent and the Banning Patent, either alone, or in combination, fail to teach or suggest *a call instruction including storing a return address to the first page of memory*. It appears that the Examiner has failed to directly address this claim limitation.

In addition, the Arora Patent and the Banning Patent, either alone, or in combination, fail to teach or suggest *a call instruction including storing the first privilege level in a previous privilege level state*. The Examiner submits that the CPL 38 is the previous privilege level state and the privilege level of the EPC instruction is the current privilege level. (Office Action, page 3). The Examiner also submits that the privilege level of the EPC instruction is the privilege level necessary for the instruction that is currently being prepared for execution in the system, thus it is a current privilege level; and that the CPL is the

previous privilege level because it was the privilege level necessary for the execution of a previous instruction. (Office Action, page 3).

The Arora Patent does not disclose a call instruction that stores the first privilege level in a previous privilege level state. Even if CPL 38 stores the previous privilege level as suggested by the Examiner, there is no call instruction that stores the privilege level in CPL 38. Based on the Examiner's interpretation, CPL 38 merely becomes the stored previous privilege level state when the EPC instruction is executed. In addition, claim 6, recites *executing application instructions in a processor of the computer system at a current privilege level of the processor equal to a first privilege level, and wherein the current privilege level controls application instruction execution in the computer system by controlling accessibility to system resources*. The current privilege level as recited in claim 6 is not the privilege level of previous instructions but rather the privilege level for currently executing instructions. Further, in the Arora Patent the CPL is never stored in a previous privilege level state. The CPL is increased when an EPC instruction is retired. (Col. 6, lines 54-56). The Arora Patent discloses a current privilege level and a privilege level of an EPC instruction (which is a *future privilege level*) as opposed to the current privilege level and the stored *previous privilege level* state as recited by claim 6.

In view of the above, Applicants believe independent claim 6 to be allowable over the Arora Patent and the Banning Patent. Dependent claims 7-11 further define patentably distinct independent claim 6. Accordingly, dependent claims 7-11 are also believed to be allowable over the Arora Patent and the Banning Patent.

The Arora Patent and the Banning Patent, either alone, or in combination, also fail to teach or suggest the computer system of independent claim 12 including **a memory having a plurality of memory pages including a first memory page storing a privilege promotion instruction, wherein the first memory page is not writeable by application instructions at a first privilege level;** and **performing the privilege promotion instruction as follows: reads the previous privilege level state; compares the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promotes the current privilege level to a second privilege level which is higher than the first privilege level.**

For similar reasons as discussed above with reference to independent claims 1 and 6, the Arora Patent and the Banning Patent, either alone, or in combination, fail to teach or suggest the above limitations of independent claim 12, which are similar to the above limitations of independent claims 1 and 6.

In view of the above, Applicants believe independent claim 12 to be allowable over the Arora Patent and the Banning Patent. Dependent claims 13-16 further define patentably distinct independent claim 12. Accordingly, dependent claims 13-16 are also believed to be allowable over the Arora Patent and the Banning Patent.

The Arora Patent and the Banning Patent, either alone, or in combination, also fail to teach or suggest the computer system of independent claim 17 including **a memory having a plurality of memory pages including a first memory page storing application instructions and a second memory page storing a higher privileged routine and a privilege promotion instruction, wherein the second memory page is not writeable by the application instructions at a first privilege level; wherein the processor executes the application instructions with the current privilege level equal to the first privilege level and the application instructions perform a call instruction to the second memory page as follows: stores a return address to the first memory page; and stores the first privilege level in a previous privilege level state; and wherein the operating system performs the privilege promotion instruction as follows: reads the stored previous privilege level state; compares the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promotes the current privilege level to a second privilege level which is higher than the first privilege level.**

For similar reasons as discussed above with reference to independent claims 1 and 6, the Arora Patent and the Banning Patent, either alone, or in combination, fail to teach or suggest the above limitations of independent claim 17, which are similar to the above limitations of independent claims 1 and 6.

In view of the above, Applicants believe independent claim 17 to be allowable over the Arora Patent and the Banning Patent. Dependent claims 18-22 further define patentably

distinct independent claim 17. Accordingly, dependent claims 18-22 are also believed to be allowable over the Arora Patent and the Banning Patent.

The Arora Patent and the Banning Patent, either alone, or in combination, also fail to teach or suggest the computer readable medium of independent claim 23 containing a privilege promotion instruction for controlling a computer system to perform a method including **reading a stored previous privilege level state; comparing the read previous privilege level state to the current privilege level; and if the previous privilege level state is equal to or less privileged than the current privilege level, promoting the current privilege level to a privilege level which is higher than the current privilege level.**

For similar reasons as discussed above with reference to independent claims 1 and 6, the Arora Patent and the Banning Patent, either alone, or in combination, fail to teach or suggest the above limitations of independent claim 23, which are similar to the above limitations of independent claims 1 and 6.

In view of the above, Applicants believe independent claim 23 to be allowable over the Arora Patent and the Banning Patent. Dependent claim 24 further defines patentably distinct independent claim 23. Accordingly, dependent claim 24 is also believed to be allowable over the Arora Patent and the Banning Patent.

Therefore, Applicants respectfully request reconsideration and withdrawal of the 35 U.S.C. § 103(a) rejection to claims 1-24, and request allowance of these claims.

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CONCLUSION

In view of the above, Applicants respectfully submit that pending claims 1-24 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-24 is respectfully requested.

No fees are required under 37 C.F.R. 1.16(h)(i). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 08-2025.

The Examiner is invited to contact the Applicants' representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Response should be directed to either Patrick G. Billig at Telephone No. (612) 573-2003, Facsimile No. (612) 573-2005 or David A. Plettner at Telephone No. (408) 447-3013, Facsimile No. (408) 447-0854. In addition, all correspondence should continue to be directed to the following address:

IP Administration
Legal Department, M/S 35
HEWLETT-PACKARD COMPANY
P.O. Box 272400
Fort Collins, Colorado 80527-2400

Respectfully submitted,
Dale C. Morris, et al.,
By their attorneys,
DICKE, BILLIG & CZAJA, PLLC
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402
Telephone: (612) 573-2003
Facsimile: (612) 573-2005

Date: 8-7-07
PGB:kmh

Patrick G. Billig
Reg. No. 38,080

CERTIFICATE UNDER 37 C.F.R. 1.8:
The undersigned hereby certifies that this paper or papers, as described herein, are being transmitted via facsimile to Facsimile No. (571) 273-8300 on this 7th day of August, 2007.

By:
Name: Patrick G. Billig